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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
KIELIN,E	
ART UNIT	PAPER NUMBER
2813	13

DATE MAILED: 06/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/346,436	Houston
Examiner	**Art Unit**
Erik Kielin	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 16, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-4, 7-9, and 12-26* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-4, 7-9, and 12-24* is/are rejected.

7) ☒ Claim(s) *25 and 26* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1**, 3, 7-9 and **18**-21, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by **Hayashi** (US 5,087,585).

Regarding claims 1 and 3, Hayashi discloses a method of fabricating an SOI structure comprising:

(a) providing a substrate 21, 22 (Fig. 2B) having at least one of active or passive elements on a surface thereof (i.e. the "first layer device" 22) and a device wafer 14, 15, 23 having at least one of active or passive elements on a surface thereof (i.e. "second layer thin film device" 23);

(b) forming an electrically insulating layer 17 having opposed faces on the surface of one of the substrate and the device wafer and having an electrical interconnect structure 18 therewithin and extending to at least one face; and

(c) bonding said electrically insulating layer to the substrate at the bond region 13, a refractory metal bump, wherein the interconnect structure 18 contacts the bond region (Figs. 2B-2C).

Regarding claims 7-9, Hayashi discloses a method of fabricating an SOI structure comprising:

providing a substrate 21, 22 (Fig. 2B), with a planar surface, having at least one of active or passive elements on a surface thereof (i.e. the "first layer device" 22); a device wafer 14, 15, 23, with a planar surface, having at least one of active or passive elements on a surface thereof (i.e. "second layer thin film device" 23); and an electrically insulating layer 17 having an electrical interconnect structure 18 therewithin and extending to a surface thereof, said interconnect structure separating a portion of said device layer from said substrate;

Regarding claims 18-21, and 23-24, Hayashi discloses a method of fabricating an integrated circuit comprising:

(a) providing a device layer 23 having devices (Fig. 2B);

(b) providing a substrate 21 having devices 22 thereon;

(c) providing a dielectric 17 bonded to one of said device layer and said substrate having an interconnect 18 disposed therein and extending to at least one surface thereof; and

(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate and forming an electrically conductive path across said interface to said interconnect.

See also columns 3-4 and column 5, lines 11-16.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1**-4, 7-9 and **18**-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi** in view of **Applicant's admitted prior art**.

Hayashi, as indicated above, discloses all of the features of the instant invention except for applying a voltage across the electrically insulating layer to break down said portion of said electrically insulating layer.

On page 7, lines 7-12, **Applicant** indicates that it is known in the art to break down oxide by applying voltage across an electrically insulating layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made because native oxide (i.e. the electrically insulating layer) inherently forms on all metals (perhaps with the exception of gold) --particularly **Hayashi's** refractory metal bump and indium metal pool-- and for the reasons indicate by **Applicant**.

Allowable Subject Matter

5. **Claims 25 and 26** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Although Applicant's specification states that it is "well known in the art" to break down an electrically insulating layer, such as a "thin native oxide" or "flowable dielectric" formed during fabrication of the interconnect, the prior art of record does not teach or suggest *intentionally forming* "an electrical insulation" over the interconnect before bonding the interconnect substrate to the device substrate and then electrically breaking down the "electrical insulation."

Response to Arguments

7. Applicant's arguments filed 5/16/01 (Amendment B, Paper No.8) have been fully considered but they are not persuasive.

Examiner notes that each of Applicant's arguments is generally constructed as a restatement of **each and every** claim with *mere allegations* that **Hayashi** fails to teach or suggest said limitations/features. Applicant has provided no substantive argument to support such allegation of absence of said features. Instead Applicant merely alleges their absence with no indication as to why said features are absent. But the body of Examiner's rejections as presented in the last two office actions (Paper Nos. 4 and 7) as well as the present office action makes clear that each of the features and/or steps is present.

For example, Applicant argues that the Hayashi interconnect 18 does not "extend substantially to the one of the outer faces of the electrically insulating structure." Figure 1E in Hayashi clearly shows such electrically insulting layer 17 with interconnect 18 "extend[ing] substantially to the one of the outer faces of the electrically insulating structure." Examiner is perplexed as to how Applicant does not see this, but provides no argument other than stating that this feature is not there.

For another example, Applicant alleges that Hayashi does not teach or suggest "a device layer having at least one of the active or passive elements on a surface thereof, a substrate having at least one of active or passive elements on a surface thereof." Not only do Applicant's figures fail to show such claimed active or passive elements, Hayashi clearly indicate in Fig. 2B a device layer 23 and a device layer 22 on a substrate 21. Examiner cannot understand what Applicant believes these "device" layers are. Clearly, they are layers with devices which are implicitly active or passive devices (elements). The Hayashi layers are certainly no different that those shown in Applicant's figures or described in Applicant's specification.

For another example, Applicant alleges that the Hayashi substrate is apparently not a semiconductor substrate but the Hayashi figures clearly states --on the figures themselves-- that the substrate 21 is silicon (Si) which is the most notoriously well known semiconductor substrate used in semiconductor fabrication today and for the past 30 years. Applicant's allegation is wholly without merit and wholly unbelievable.

Taken as a whole Applicant's arguments are wholly without merit. When features which are most clearly present in Hayashi are merely alleged to be absent by Applicant without any supporting argument, it is not possible for Examiner to address the allegations beyond referring to the rejections above wherein each of the features alleged absent by applicant is in fact present in Hayashi.

Regarding claim 1, Applicant argues that "[t]here is no build-up of layer upon layer as is found in Hayashi." Examiner respectfully disagrees noting that, not only does Applicant build up layers in the claim at issue in order to form the electrically insulating layer on either of the surfaces of either of the device wafer or the substrate, Hayashi discloses this same claimed step. Ergo, Hayashi builds up layers only to the extent that Applicant does. Therefore, Applicant's argument is wholly without merit.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rioult (US 3,787,822) teaches applying a voltage across a dielectric interface 16 between conductive metal layers 12, 15 interface to remove native metal oxide from interconnect material (Abstract).

Buti et al. (US 5,260,233) anticipates Applicant's claimed invention except for the admittely known electrical breakdown of the native oxide layer.

Davidson (US 5,880,010) anticipates Applicant's claimed invention except for the admittely known electrical breakdown of the native oxide layer.

Kelly et al. (US 6,183,588 B1) anticipates Applicant's claimed invention except for the admittely known electrical breakdown of the native oxide layer.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication from examiner should be directed to Erik Kielin whose telephone number is (703) 306-5980 and e-mail address is erik.kielin@uspto.gov. The examiner can normally be reached by telephone on Monday through Thursday 9:00 AM until 7:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached at (703) 308-2417 or by e-mail at charles.bowers@uspto.gov. The fax phone number for the group is (703) 308-7722 or -7724.

EK

June 1, 2001

Charles Bowers
Supervisory Patent Examiner
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